REMARKS

The Office Action mailed November 16, 2004 has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-20 were pending. Claims 1, 2, 3, 11, 15, and 20 were rejected. Claims 3-10, 12-14, and 16-19 were objected to, but were identified as being allowable if re-written in independent form. In this paper, Claim 20 is amended, and new Claim 21 is added. Claims 1-21 are currently pending. No new subject matter has been added. For at least the following reasons, Applicant respectfully submits that each of the presently pending claims is in condition for allowance.

Objection to the specification

The title was objected to. It is respectfully submitted that the objection to the title is moot in light of the amendment to the title.

Rejection under 35 U.S.C. § 102(b)

Claims 1, 2, and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yamashita et al. (US-5,281,865).

The rejection to Claims 1 and 2 is respectfully traversed.

It is respectfully submitted that Claim 1 is allowable at least because Yamashita does not disclose "a first switch circuit that is coupled between the first switch node and the second multiplexer output node", as recited in Applicant's Claim 1.

The Office Action stated that the switch circuits recited in Applicant's Claim 1 read on inverters 1104 and 1103 of FIGURE 11A in the Yamashita reference. Applicant respectfully disagrees. Since inverters 1104 and 1103 do not "open", they are not switch circuits.

Claims 2-10 and 21 are submitted to be allowable at least because they depend on Claim 1, which is proposed to be allowable.

It is respectfully submitted that the rejection to Claim 20 is moot in light of the amendment to Claim 20. Claim 20 is submitted to be allowable at least because Yamashita does not disclose "substantially isolating the first inverted signal from the second multiplexer output node", as recited in Applicant's Claim 20 as amended.

Rejection under 35 U.S.C. § 103(a)

Claims 11 and 15 were rejected under 35 U.S.C. § 103(a) as being anticipated by Yamashita et al. (US-5,281,865). The rejection is respectfully traversed.

First, Claim 11 is submitted to be allowable because Yamashita does not teach or suggest all of the limitations of Applicant's Claim 11.

Argument 1: Switch circuits

In particular, Yamashita does not teach or suggest the switch circuits recited in Applicant's Claim 11. It is respectfully submitted that inverters 1104 and 1103 of FIGURE 11A of Yamashita are not switch circuits.

Argument 2: Multiplexer circuit

Additionally, Yamashita does not teach or suggest the limitation "multiplexer circuit", as recited in Applicant's Claim 11. The Office Action states that master latch 1110 is a "a type of MUX because it performs the function of selecting, as output, either signal MB or MT which corresponds to the inverse of inputs DT or DB respectively, in essentially the same manner in applicant's Fig. 4."

Applicant respectfully disagrees. Signals DT and DB from the Yamashita reference are complementary signals (see column 11, lines 27-29 of Yamashita). Master latch 1110 in FIG. 11A of Yamashita is identical to the circuit of FIG. 1A of Yamashita, except that outputs QB and QT of FIG. 1A in Yamashita become MB and MT in FIG. 11A (see column 11, lines 22-24 of Yamashita), and CK is used in master latch 1110 instead of CKB of FIG. 1A. FIG. 1B of Yamashita shows the truth table for the circuit of FIG. 1A of Yamashita. Based on the truth table in FIG. 1B of Yamashita, for master latch 1110, if CK is high, MT and MB are both high-impedance. If CK is low, MT is the same as DT and MB is the same as DB. Master latch 1110 of Yamashita does not "select" between DT and DB. Furthermore, there is no reason to "select" between DT and DB of Yamashita, since they are complementary signals. The output is not even defined for the case where DT and DB of Yamashita both have the same logic level.

Argument 3: Unsatisfactory for intended purpose

Further, the modification proposed by the Office Action, of using master latch 1110 of Yamashita in a place of a latch or multiplexer in a typical column driver, would render the column driver **unsatisfactory for its intended purpose**. For example, in the proposed combination, if master latch 1110 of Yamashita received one input as a logic high within column zero, and another input as a logic high within column one, the output of master latch 1110 would be undefined (see FIG. 1B of Yamashita, the output is not defined for both inputs being high). Accordingly, the column driver would not function properly in the proposed combination.

For at least the reasons stated above, Claim 11 is respectfully submitted to be allowable, and notice to that effect is respectfully requested. Claims 12-19 are respectfully submitted to be allowable at least because they depend on Claim 11, which is proposed to be allowable.

Conclusion

It is respectfully submitted that each of the presently pending claims (Claims 1-21) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicants' representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicants reserve the right to raise these arguments in the future.

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Respectfully submitted,

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